REMARKS

Reconsideration of all grounds of objection and rejection, and allowance of all the pending claims are respectfully requested in light of the above amendments and the following remarks. Claims 1-4, 12 amended, remain pending herein.

The Abstract has been edited to overcome the objections in the Office Action.

Figures 1 and 2 have been amended to contain the legend of "Prior Art".

Claims 1-4 stand rejected under 35 U.S.C. §112, second paragraph. Claims 1-4 stand rejected under 35 U.S.C. §102(b) in view of Applicant's Prior Art shown in FIG. 2. Claim 1 stand rejected under 35 U.S.C. §102(b) in view of Wang (U.S. 6,166,571). Applicant respectfully traverses all of these grounds of rejection for the reasons indicated herein below.

With regard to the rejections under 35 U.S.C. §112, second paragraph, Applicant has amended claims 1-4 in accordance with the Examiner's rejections. More specifically, with regard to claim 2, Applicant respectfully submits that the "inverter stage" was changed to the second inverted output of the second flip-flip M1', M2', M3', M4', and is fully supported by FIGs. 3 and 4.

With regard to the rejections under 35 U.S.C. 102(b) in view of Applicants Prior Art FIGs. 1 and 2, Applicant respectfully submits that claim 1 has been amended to recite in part:

> second flip-flop having a second clock input for receiving a second clock signal that is substantially in anti-phase with the clock signal inputted into the first clock input, a second set input coupled to the first non-inverted output, a second non-inverted output and a second inverted output, wherein the second inverted output beingis coupled to the first set input for providing an inverted

output signal from the second flip-flop as feedback to the set input of the first flip-flop.

Support for the above amendment to claim 1 is clearly shown in FIGs. 3 and disclosed in the specification at paragraph [0008] , and paragraph [0018].

The frequency divider recited in claim 1 eliminates a controlled inverter comprising a pair of transistors (M5, M6) shown in the prior art of FIGs. 1 and 2, by having the second flip-flop having "the second inverted output is coupled to the first set input for providing an inverted output signal from the second flip-flop as feedback to the first flip-flop" (please see FIG. 3 and paragraph [0008] and [0018]).

In prior art FIGs. 1 and 2, the second flip-flop is not arranged such that an inverted output is fed back to the first flip-flop, but instead has ***a non-inverted output*** *of the second flip-flop Q2 connected to inverter M5, M6, which is then output as signal Q4 to the first flip-flip).*

In contrast, the structure as recited in claim 1 eliminates the required inverter M5 and M6 and does not suffer the delay introduced by M5 and M6 of the prior art of FIGs. 1 and 2. The frequency divider as recited in claim 1 permits an increase in the maximum frequency of input signals.

For at least the above reasons, Applicant respectfully submits that claims 1-4 are not anticipated by prior art FIGs. 1 and 2, as these FIGs. fail to disclose a structure as claimed. Nor would any of the present claims have been obvious as being within the ordinary level of skill in the art.

With regard to the rejection of claim 1 under 35 U.S.C. §102(b) in view of Wang, Applicant also respectfully submits that this claim is not anticipated by Wang. The flip-

flops shown in Wang clearly have stacked transistors Q10, Q20, Q100, and Q30, Q40, Q200, which suffer from the same problems disclosed by the Applicant at paragraph [0004], last 8 lines.

In contrast, present claim 1 has been amended to recite in part a first flip-flop without stacked transistors, and a second flip-flop without stacked transistors, with support clearly shown in FIGs. 3 and 4.

Present claim 1 thus recites structure that is not anticipated by Wang (or prior art FIGs. 1 and 2 for that matter), and also provides the advantage of being suitable for operation at low voltages, which is a drawback of stacked transistor arrangements such as Wang (paragraphs [0004] and [0005]).

In accordance with MPEP 2131, under 35 U.S.C. §102, according to the United States Court of Appeals for the Federal Circuit, a "claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" (*Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (emphasis added)). Therefore, to reject a feature, which is alleged to patentably distinguish the claim containing such feature, as being anticipated by a prior art, the Office Action must establish that the same feature is present in the prior art reference. As both FIGS. 1, 2 (and Wang) fail to disclose each and every element as set forth in claims 1-4, these claims are not anticipated. Nor would any of claims 1-4 have been obvious at the time of invention as being within the ordinary level of skill in the art (*KSR International v. Teleflex*, 127 S.Ct. 1727, 82 USPQ2d 1385 (2007)).

For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Respectfully submitted,

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